* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
The manufacture approach conventional technique of the matrix which consists of the thin film transistor for a liquid crystal display which especially has a:Si-H as a semi-conductor This invention relates to the manufacture approach of the matrix which consists of the thin film transistor for a liquid crystal display which especially has a:Si-H as a semi-conductor.
Two or more approaches for manufacture of the a:Si-H form thin film transistor matrix for a liquid crystal display are common knowledge until now. These approaches usually need the mask step of five - 7 times of photolithographies. Negatives are exposed and developed, spreading of a photoresist and this photoresist rank second, and each photolithography step of these approaches means an etching process. Not only product cost but the yield determines the number of process steps. Furthermore in each lithography step, an unescapable defect occurs.
Advantage of this invention The approach of this invention of having the configuration of claim 1 given in description partial enables manufacture of the thin film transistor matrix for a liquid crystal display by only 3 times of resist steps, and the thin film transistor which has the display which moreover has almost no pixel defect, and the high mobility of a charge carrier is obtained. Furthermore, this approach can realize the high yield. It is several fusion of a process step and a lift-off step (lift-off step) according [this invention] to the double exposure of the photoresist film fundamentally.
It is alike and is based. In this lift-off step both, a photoresist and passivation are removed in the field of contact. By the process step of the small count of the approach of this invention, the yield at the time of liquid crystal display manufacture becomes very high. Saving of the production time and the machine which become shorter, and a use raw material enables advantageous manufacture in cost, and this advantageous manufacture in cost is reflected also in a product price. When the number of process steps furthermore decreases more, the load to a perimeter environment is reduced rather than the case of the conventional approach. A pixel electrode is arranged on a direct substrate, therefore is divided, and is structured simply.
The means which makes possible the advantageous amelioration implementation gestalt of an approach according to claim 1 is indicated by the subordination claim.
For example, sputtering of the indium tin oxide (ITO) is carried out on the glass substrate which is not structured yet as transparence electric conduction film for a pixel electrode. A pixel defect becomes merely small by easy structuring of ITO connected with this. as line contact and gate contact -- advantageous -- titanium -- or -- otherwise, sputtering of the tantalum-molybdenum alloy is carried out. Structuring of the ITO film and the titanium film is advantageously performed on a wet chemistry target.

The further advantage produces a-Si:H as a semi-conductor by using SiNx as a gate insulating material at sequence by making it deposit in a PECVD system within a vacuum by considering n+a-Si:H as a drain and source contact, and structuring by plasma etching. By making the film of these single strings deposit, high mobility, small breaking current, a small cut off region, slight threshold voltage, and the high thin film transistor that has electric and thermal stability are obtained, without interrupting a

vacuum.
To metallic coating of a train, a drain, and source contact, sputtering of the molybdenum film or the titanium film is carried out, and it is structured by wet chemical etching, for example. To contact, advantageously, sputtering of the aluminum is carried out and it is similarly etched into a wet chemistry target. Other metals with an obvious thing can be used for metallic coating.
Drawing A series of processes of the advantageous operation gestalt of this approach are shown in the drawing, and it is explained in detail in the following description.
Drawing 1 a-c shows the sectional view of the pixel of the liquid crystal display in the multiple-processes step for structuring gate oxide and a pixel electrode.
Drawing 2 a-f shows the sectional view which ****s in drawing 1 of the pixel in various process steps for structuring of metallic coating of a train, a drain and source contact, the dope semi-conductor film, and the intrinsic-semiconductor film.
Drawing 3 a-c shows the sectional view which ****s in drawing 1 of the pixel in various process steps for structuring of metallic coating of contact, and passivation.
Description In the coater which has the target which continues in order advantageously, the indium-tin-oxide film (ITO) 11 and the titanium film 12 are put on the glass substrate 10, and, subsequently the photoresist film 13 is applied to drawing 1 a. Next, the mask for structuring of the gate oxide of the next thin film transistor TFT and the pixel electrode of Pixel BP is exposed and developed. After this, first, the titanium film 12 is etched into a wet chemistry target by switch of an etching medium in equipment [film / 11 / ITO] next, and the structure shown in drawing 1 b as a result is acquired. The wet chemical etching of exposure and development of an ITO mask, and the titanium film 12 in the field of Pixel BP and the structure after removal of a photoresist are shown in drawing 1 c. The 1st resist step is completed by this.
The 2nd resist step is explained by drawing 2 . A series of film which consists of SiNx, a-Si:H, and n+-a-Si:H in a vacuum by the PECVD approach accumulates, and, subsequently sputtering of the molybdenum is carried out as metallic coating of a train, a drain, and source contact on the film of these single strings as first shown in drawing 2 a. Then, the photoresist film 13 is again applied to the whole substrate. Drawing 2 b)
Then, the structure after exposure and development of a gate oxide mask and a semi-conductor mask, and the wet chemical etching of the molybdenum film 17 is shown. As for drawing 2 d, the structure after plasma etching of n dope semi-conductor 16, an intrinsic semiconductor 15, and gate oxide 14 is shown. It remains, while the semi-conductor channel of a thin film transistor TFT had been covered with the molybdenum film 17. In the process step shown in drawing 2 e, in the field of a semi-conductor channel, the molybdenum film 17 is etched into a wet chemistry target, and, subsequently to n dope semi-conductor film 16 and a partial target, the non dope semi-conductor film 15 is etched at a plasma-etching step. Subsequently, a photoresist 13 is removed and the structure shown in drawing 2 f as a result arises.
Drawing 3 shows the 3rd resist step. In the approach phase shown in drawing 3 a, sputtering of the aluminum film 18 is carried out to the whole front face, and, subsequently the photoresist film 13 is applied. In this case, the aluminum film 18 and the photoresist film 13 have extended also after the contact which was being omitted in order to make it intelligible in drawing 1 and drawing 2 . Drawing 3 b shows the structure after the wet chemical etching of exposure and development of the mask for contact and the contact finger KF in the field of Pixel BP, and the aluminum film 18. subsequently, it is shown in drawing 3 c -- as -- the surface whole -- transparence passivation -- SiNx19 is put advantageously. Then, in a lift-off step, it is removed with the passivation 19 to which the photoresist 13 of the contact finger KF and the field of contact exists on these. The completed structure which is shown in drawing 3 d by this is acquired.

[Translation done.]